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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SELLERS, DANIEL R	
ART UNIT	**PAPER NUMBER**
2644	

DATE MAILED: 10/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,235	KITAMURA, MAMORU	
	Examiner	Art Unit	
	Daniel R. Sellers	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed August 01, 2005 with respect to claims 1, 2, 5-9 have been fully considered but they are not persuasive.

2. Regarding claim 1, Chatterjee teaches two control loops for controlling the pulse width modulation signals found on the two power rails. Both loops create signals that are fed forward through the system and both loops use feedback to further control the PWM signal. Chatterjee teaches all the claimed features of claim 1.

3. Regarding claim 2, Carver also has two control loops that supply the positive and negative supplies to an amplifier (Fig. 5, unit AA1). It is well known in the art of electronics that the symbol designated by AA1 comprises clockwise from the upper-left a positive input, a positive supply, an output, a negative supply, and a negative input. The upper portion of the figure comprised of components 220, 222, 224, and 226 is the first loop, wherein the signal that is the positive power signal supplied to item AA1 is fed-back to the component 220. This loop also feeds forward the signal designated by item 210A. The lower portion is a mirror image of the top part, and it supplies the negative power signal to item AA1. Carver teaches the features of claim 2.

4. Regarding claims 5 and 6, Carver does teach a triangular wave for clock generation (Col. 16, lines 23-27), wherein Carver shows a more detailed schematic with regard to this teaching (Figs. 9A and 9B). Carver, as stated above, controls the positive and negative power supplies for the amplification means. Regarding inherency, the office retracts these statements, but asserts that it would have been obvious to combine

these features in a class-D amplifier. Even though a class-D amplifier is not claimed, a class-D amplifier with the features of Carver and Kohdaka reads on the limitations of the claims as shown in the following.

5. Regarding amended claim 7, see the following rejection under 35 USC 103(a).

6. Regarding claims 8 and 9, the claim language does not refer to a digital input signal, therefore Carver teaches the claimed features of the invention.

7. Applicant's arguments, see pages 13-14 with respect to the rejection(s) of claim(s) 3 and the dependent claim 4 under 35 USC 102(e) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of well-known techniques in the art.

Claim Rejections - 35 USC § 102

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claim 1 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chatterjee et al., U.S. Patent No. 5,898,340 (hereinafter Chatterjee).

10. Regarding claim 1, see Chatterjee

An audio reproducing apparatus for amplifying an audio signal according to a pulse width modulation signal generated based on a digital audio signal and further filtering the audio signal so as to output an analog audio signal, the apparatus comprising:

a first control loop for feeding back a source voltage supplied to amplification means for amplifying the audio signal to a supply control portion of a power source for amplification and compensating a pulse width of a control signal for controlling supply of the power source for amplification; (Col. 5, lines 30-39 and Fig. 1, units 105 and 209) *and*

a second control loop for feeding forward the pulse width modulation signal to the supply control portion of the power source for amplification to compensate the pulse width of the control signal. (Col. 5, lines 40-50 and Fig. 1, units 108 and 211-213).

Chatterjee teaches these two control loops.

11. Claims 2 and 8-9 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Carver, U.S. Patent No. 6,104,248.

12. Regarding claim 2, see Carver

An audio reproducing apparatus for amplifying an audio signal according to a pulse width modulation signal generated based on a digital audio signal and further filtering the audio signal so as to output an analog audio signal, the apparatus comprising:

a first control loop for feeding back a source voltage supplied to amplification means for amplifying the audio signal to a supply control portion of a power source for amplification; (Col. 6, lines 51-59 and Fig. 5, units 220-226A) *and*

a second control loop for generating a signal of approximately the same amplitude as the variation of the source voltage supplied to the amplification means and of an opposite phase based on the pulse width modulation signal and feeding the signal forward to the supply control portion of the power source for amplification, wherein the first and second control loops are used to control the supply of the power source for amplification. (Col. 1, lines 38-49, Col. 7, lines 33-45 and Fig. 5, units 230-236A)

Carver teaches an amplifier with these features.

13. Regarding amended claim 8, see the preceding argument with respect to claim 2. Carver teaches an amplifier with these features.

14. Regarding claim 9, see the preceding argument with respect to claim 2. Carver teaches an amplifier with these features.

Claim Rejections - 35 USC § 103

15. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

16. Claims 3, 4, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carver and well-known techniques in audio reproduction.

17. Regarding amended claim 3, see Carver figure 5 and figure 9A, unit 340, items R77 and C36. Carver teaches an amplifier with these features, however Carver utilizes an analog audio input signal to create the PWM signals. It is well known in the art of audio reproduction and the Office takes Official Notice that it is well known to connect a digital audio component such as a CD player to an analog amplifier, wherein the CD player reads a digital signal from the CD and converts it to analog for amplification. It would have been obvious for one of ordinary skill in the art at the time of the invention to combine the teachings of Carver and the well-known art for the purpose of amplifying signals read from a music CD.

18. Regarding claim 4, the further limitation of claim 3, see Carver

... wherein the power source supply control means is a switching regulator for exerting control to intermittently supply power from the power source for amplification to the amplification means according to the predetermined control signal; and (Col. 20, line 64 – Col. 21, line 6 and Fig. 5, units 226 and 236)

wherein the compensation means compensates the pulse width of the predetermined control signal based on the feedback-inputted and feedforward-inputted signals. (Fig. 5, units 210, 210A, 210B, 212, 220-226A, and 230-236A)

Carver teaches an amplifier with these features.

19. Regarding claim 7, see Carver

An audio reproducing apparatus for amplifying an audio signal according to a pulse width modulation signal generated based on a digital audio signal and further filtering it so as to output an analog audio signal, the apparatus comprising:

means for detecting a source voltage supplied to amplification means for amplifying the audio signal; and (Fig. 5, unit 220)

feedback means for feeding the source voltage back to a supply control portion of a power source for amplification so as to compensate a pulse width of a control signal for controlling supply of the power source for amplification based on the source voltage fed back. (Fig. 5, unit 220, items R1 and R2)

Carver teaches an amplifier with these features, and it is obvious to include a digital music source as stated previously with regard to claim 3.

20. Claims 5, 6, and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Carver and Kohdaka et al., U.S. Patent No. 5,245,345 (hereinafter Kohdaka).

21. Regarding claim 5, see Carver

An audio reproducing apparatus, comprising:
–; modulation means for performing a conversion process based on –; modulation to an inputted digital audio signal and generating a pulse width modulation signal;
amplification means for amplifying the audio signal based on the pulse width modulation signal generated by the –; modulation means;
filter means for filtering a signal outputted from the amplification means and generating an analog audio signal; (Fig. 9A, unit 340, items R77 and C36)
power source supply control means for controlling supply of a power source for amplification to the amplification means according to a predetermined control signal; (Fig. 5, units 212 and 226)
triangular wave generation means for generating a triangular wave signal based on a predetermined clock signal; (Col. 3, lines 11-19 and Fig. 5, unit 212)
signal generation means for generating a signal of approximately the same amplitude as the variation of a source voltage supplied to the amplification means and of the opposite phase based on the pulse width modulation signal generated by the –; modulation means; (Fig. 5, units 210, 210A, 210B, 220-226A, and 230-236A)
first comparison means for inputting to one input terminal the signal of the amplitude according to the source voltage supplied to the amplification means and inputting, to the other input terminal, the signal from the power source for amplification and the signal generated by the signal generation means so as to compare the two input signals and generate a difference signal; and (Fig. 5, unit 220, 230, Fig. 9A, unit 330 and Fig. 9B, unit 320)
second comparison means for inputting to one input terminal the triangular wave signal generated by the triangular wave generation means and inputting to the other input terminal the difference signal outputted from the first comparison means so as to compare the two input signals, generate the predetermined control signal and supply the predetermined control signal to the power source supply control means. (Fig. 5, units 222 and 232, Fig. 9A, unit 332, and Fig. 9B, unit 322)

Carver teaches an amplifier with the features as shown above. Carver does not teach a class D amplifier for use with the tracking power supply. However, it would have been obvious that the PWM used in the tracking power supply could have been used to create a class D amplifier, as shown in the prior art (Fig. 2), for the purpose of creating a more efficient power stage. Carver also does not teach the delta-sigma modulation means or the conversion means. Kohdaka teaches a digital-to-analog converter (DAC), which employs delta-sigma modulation means and a conversion means (Col. 1, lines

52-65 and Col. 3, lines 49-51). Kohdaka's system does not teach an output stage for amplification, but it would have been obvious in the creation of a PWM signal that a class D amplification stage would be used for subsequent amplification for the purpose of better efficiency. It would have been obvious for one of ordinary skill in the art to combine the teachings of Carver and Kohdaka for the purpose of higher fidelity in a class D amplifier with a digital input.

22. Regarding claim 6, see the preceding argument with respect to claim 5. The combination of Carver and Kohdaka teaches these features.

23. Regarding claim 10, see the preceding argument with respect to claim 5. Kohdaka teaches the DAC which outputs a PWM signal. Carver teaches a driver circuit (see Fig. 9b, unit 324), an amplifier circuit responsive to the PWM signal (Fig. 9a, unit 340), and a compensation circuit with the difference amplifier (Fig. 9b, unit 320), the feedback loop (Fig. 9b, bottom most trace that connects the output of the unit 326 to an input of unit 320), a feed forward signal in the loop (Fig. 9b, unit 322), a voltage supply (Fig. 9a, unit 302 and Fig. 9b, unit 320, +10 signal), and a comparator (Fig. 9b, unit U3A). Carver teaches that the control signal controls the power source of the amplifier.

24. Regarding claim 11, the further limitation of claim 10, see Carver column 16, lines 23-27. Carver teaches that the reference signal from clock (312) is a triangular wave.

25. Regarding claim 12, the further limitation of claim 10, see the preceding argument with respect to claim 2. Carver shows a control loop that has essentially the same amplitude but opposite phase for generating the negative power supply signal.

26. Regarding claim 13, the further limitation of claim 10, see the preceding argument with respect to claim 10. Carver teaches a comparator within the PWM signal generation means, wherein the output is compensated by the feedback loop.

27. Regarding claim 14, the further limitation of claim 13, see the preceding argument with respect to claim 10 and see Carver column 5, lines 5-11. Carver teaches that the amplifier supply voltage is compensated.

28. Regarding claim 15, the further limitation of claim 13, see the preceding argument with respect to claim 10. Kohdaka teaches a DAC with a low pass filter, wherein an analog signal is output from. In the combination, Kohdaka's DAC would provide the analog input to Carver's amplifier, so there would be no feedback to the DAC in the combination.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Robert W. Carver, U.S. Patent No. 4,218,660, Farrington et al., U.S. Patent No. 5,912,549, and Meir Shashoua, U.S. Patent No. 6,373,340.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel R. Sellers whose telephone number is 571-272-7528. The examiner can normally be reached from Monday to Friday, 9am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian Chin can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DRS

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